



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nowak et al.

Serial No.: 10/604,086

Filed: June 25, 2003

Title: Method of Making a finFET Having  
Suppressed Parasitic Device Characteristics

IBM Docket No.: BUR920030005US1  
(02016-00153)

Group Art Unit: Not yet assigned

Examiner: Not yet assigned

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING (37 C.F.R. 1.8a)

I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, Alexandria, VA 22313-1450.

*Morgan S. Heller II* 7/02/03  
Morgan S. Heller II Date

July 2, 2003

Supplemental Information Disclosure Statement Transmittal

In connection with the above-identified application, please find attached a Supplemental Information Disclosure Statement and copies of the references cited therein.

Respectfully submitted,

DOWNS RACHLIN MARTIN PLLC

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BTV/245689.1

P242-12/00

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**INFORMATION DISCLOSURE STATEMENT FILED PURSUANT TO THE  
DUTY OF DISCLOSURE UNDER 37 C.F.R. §§1.56, 1.97 AND §1.98**

Pursuant to the duty of disclosure under 37 C.F.R. §§1.56, 1.97 and §1.98, applicants request consideration of this Information Disclosure Statement.

Information Cited

Applicants hereby make of record in the above-identified application the information listed on the attached form PTO-1449 (modified). The order of presentation of the references should not be construed as an indication of the importance of the references.

REMARKS

A copy of each of the above-identified items of information is enclosed unless otherwise indicated on the attached form PTO-1449 (modified). It is respectfully requested that:

1. the examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;
2. the enclosed form PTO-1449 be signed by the examiner to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application; and
3. the citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, applicants make no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, applicants make no representation that the information cited in this Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).


By submitting this Information Disclosure Statement, applicants make no representation that the information cited in this Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. §102.

Notwithstanding any statements by applicant, the examiner is urged to form his/her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

Respectfully submitted,

DOWNS RACHLIN MARTIN PLLC

By:   
Morgan S. Heller II  
Reg. No. 44,756  
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FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT

Page 1 of 1

(Use several sheets if necessary.)

ATTY DOCKET NO.  
BUR920030005US1

SERIAL NO.  
10/604,086

APPLICANT:  
Nowak et al.

FILING DATE:  
June 25, 2003

GROUP:  
Not yet assigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA						
	AB						
	AC						

U.S. PATENT APPLICATION PUBLICATIONS

	AD						
	AE						
	AF						
	AG						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AH	EP0763851	19.03.1997	Europe				

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AI	<i>A Bulk-Si-compatible Ultrathin-body SOI Technology for sub-100nm MOSFETs</i> ; V. Subramanian, J. Kedzierski, N. Lindert, H. Tam, Y. Su, J. McHale, K. Cao, T-J. King, J. Bokor, & C. Hu; Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA; date unknown.
	AJ	<i>A Folded-channel MOSFET for Deep-sub-tenth Micron Era</i> ; Digh Hisamoto, wen-Chin Lee, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Kazuya Asano, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu; Central Research Laboratory, Hitachi Ltd., EECS, UC Berkley, Lawrence Berkeley Laboratory, Nippon Steel Corp, NKK Corp.; 0-7803-4777-3/98 - 1998 IEEE
	AK	<i>Sub 50-nm FinFET: PMOS</i> ; Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor and Chanming Hu; Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA; 0-7803-5413-3/99; 1999 IEEE
	AL	<i>A Fully Depleted Lean-Channel Transistor (DELTA) - A Novel Vertical Ultrathin SOI MOSFET</i> ; Digh Hisamoto, Toru Kaga, Yoshifumi Kawamoto and Edi Takeda; IEEE Electron Device Letters, Vol. 11, No. 1, January 1990; 0741-3106/90/0100-0036\$01.00.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

P270 - 02/03  
BTV/245438.1